

02-404

PTO/SB/21 (08-03)

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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/668,467
	Filing Date	September 23, 2003
	First Named Inventor	Sachin Mullick
	Art Unit	2328
	Examiner Name	
Total Number of Pages in This Submission	Attorney Docket Number	10830.0100.NPUS00

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Firm or Individual name	Howrey Simon Arnold & White, LLP	
Signature	<i>Richard C. Auchterlonie</i> Reg. 30,607	
Date	February 23, 2004	

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Form PTO-1449 (modified)

Atty. Docket No.

10830.0100.NPUS00

Serial No.

10/668.467

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

Applicant

Sachin Mullick, Jiannan Zheng, Xiaoye Jiang,
Sorin Faibish, Peter Bixby

Filing Date:

09/23/2003

Group:

2157

(Use several sheets if necessary)

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date of App.
	A1	6,434,681	8/13/2002	Armangau	711	162	12/2/1999
	A2	6,324,581	11/27/2001	Xu et al.	709	229	3/3/1999
	A3	6,279,011	8/21/2001	Muhlestein	707	204	6/19/1998
	A4	6,269,431	6/31/2001	Dunham	711	162	8/13/1998
	A5	6,076,148	6/13/2000	Kedem	711	162	12/26/1997
	A6	5,963,962	11/5/1999	Hitz et al.	707	202	6/30/1998
	A7	5,915,264	6/22/1999	White et al.	711	168	4/18/1997
	A8	5,893,140	11/13/1996	Vahalia et al.	711	118	11/13/1996
	A9	5,835,953	11/10/1998	Ohran	711	162	11/8/1996
	A10	5,819,292	10/6/1998	Hitz et al.	707	203	5/31/1995
	A11	5,701,516	12/23/1997	Cheng et al.	395	842	1/19/1996
	A12	5,379,412	1/3/1995	Eastridge et al.	395	575	4/20/1991
	A13	5,375,232	12/20/1994	Legvold et al.	395	575	9/23/1992
	A14	5,218,695	6/8/1993	Noveck et al.	395	600	2/5/1990
	A15	5,175,852	12/29/1992	Johnson et al.	395	600	11/4/1989
	A16	5,175,837	12/29/1992	Arnold et al.	395	425	2/3/1989
	A17	5,155,845	10/13/1992	Beal et al.	395	575	6/15/1990

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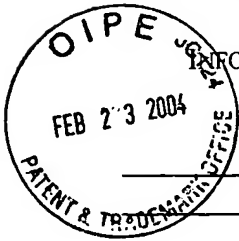
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Other Art (Including Author, Title, Date Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C1	EMC Celerra SE5 File Server, EMC Corporation, Hopkinton, Mass. 01748-9103, 2002, 2 pages.
	C2	"Celerra File Server in the E-Infostructure," EMC Corporation, Hopkinton, Mass., 2000, 9 pages.
	C3	"Celerra File Server Architecture for High Availability," EMC Corporation, Hopkinton, Mass., August 1999, 7 pages.
	C4	Chutani, Sailesh, et al., "The Episode File System," Carnegie Mellon University IT Center, Pittsburgh, PA, June 1991, 18 pages.
	C5	Vahalia, Uresh, <u>UNIX Internals: The New Frontier</u> , Chapter 9, "File System Implementations," Prentice Hall, Inc., Upper Saddle River, New Jersey, pp. 261-289.
	C6	Helen S. Raizen and Stephen C. Schwarm, " <i>Building a Semi-Loosely Coupled Multiprocessor System Based on Network Process Extension</i> ," Pre-publication copy 1/29/1991 (To be published by 1991 USENIX Symposium on Experiences with Distributed & Multiprocessor Systems), pp. 1-17.
	C7	Miruja et al., " <i>Design and Evaluation of the High Performance Multi-Processor Server</i> ," Proceedings - IEEE International Conference on Computer Design: VLSI in Computers and Processors; Cambridge, Mass. Oct. 10-12, 1994, 1063-6404/94, 1994, IEEE, pp. 66-69.
	C8	" <i>Intel® Xeon™ Processor: Unparalleled Value and Flexibility for Small and Medium Business Server Applications</i> ," 2002, Intel Corporation (4 pages).
	C9	" <i>Intel® Server Board SE7500WV2: Superior Performance for Reliable and Manageable High-Density Solutions</i> ," 2002, Intel Corporation (6 pages).
	C10	" <i>Building Cutting-Edge Server Applications; Intel® Xeon™ Processor Family Features the Intel NetBurst™ Microarchitecture with Hyper-Threading Technology</i> ," 2002, Intel Corporation, pp. 1-9.
	C11	" <i>Intel® Pentium® 4 and Intel® Xeon™ Processor Optimization</i> " Reference Manual, 2002, Intel Corporation, U.S.A., pp. i to xxv, 1-1 to 1-27, 2-1 to 2-75, 7-1 to 7-33.
	C12	Hennessy, John L., and Patterson, David A., <u>Computer Architecture: A Quantitative Approach</u> , Morgan Kaufmann Publishers, Inc., San Mateo, CA, 1990, pp. 250-284.

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10830.0100.NPUS00Serial No.
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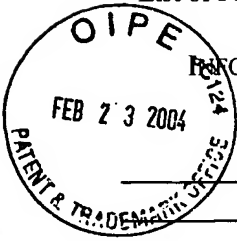
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Other Art (Including Author, Title, Date Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C13	Troiani, Mario et al., "The VAX 8600 I Box, A Pipelined Implementation of the VAX Architecture," <u>Digital Technical Journal</u> , No. 1, Aug. 1985, pp. 24-42.

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